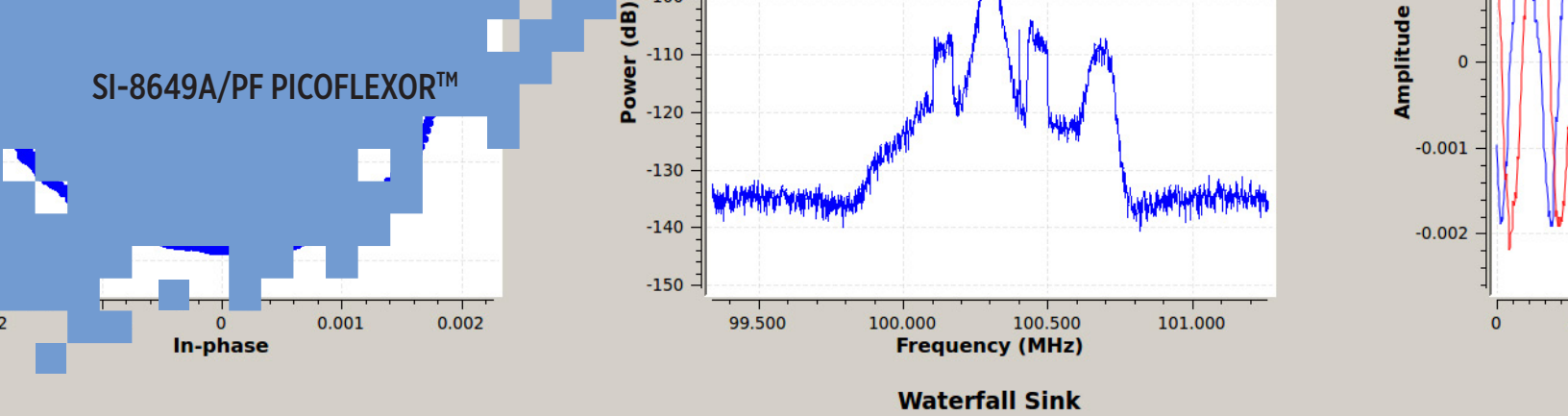


SI-8649A/PF PICOFLEXOR™



PICOFLEXOR: MINIATURE SIGINT SOFTWARE DEFINABLE RADIO (SDR) PLATFORM

PicoFlexor™ is a miniature software definable radio (SDR) platform **designed for both application development and deployment** in the field. It combines the **high RF performance of the Picoceptor™**, state-of-the-art digital processing, and a simple development interface to create a best-in-class SIGINT SDR solution.

Its software-definable architecture means that it can be deployed for a signal intercept/analysis application, then re-deployed for threat warning/situation awareness, and again re-deployed to other mission-critical applications, such as precision geo-location or modern signal analysis.

PicoFlexor is designed to rapidly leverage power reduction and performance gains of next-generation digital technology. The **architecture is optimized to integrate with open SDR standards such as RedHawk and GNURadio.**

PicoFlexor is available in **single and dual RF channel configurations.** It is **phase coherent for N-channel**

applications by distributing the reference from a master unit to slave units. Its **precision timing capability supports geolocation applications.** All **mission-specific data is stored on a removable micro-SD card.**

Optional **Aft-End-Peripherals provide various I/O standards via a high-speed backplane.** A unified tool interface is used for FPGA and software development. A common application program interface (API) enables rapid porting of designs across digital technologies. PicoFlexor's digital roadmap includes the Xilinx 7-series FPGA and beyond.



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PERFORMANCE FEATURES

PARAMETER	SPECIFICATION
Tuning Range	2 MHz - 3 GHz 2 MHz - 12.4 GHz with SI-9249/FE12
Channels	Single or Dual
Bandwidth	6 MHz or 25 MHz
Digital drop receiver	Two channels
Digital receiver bandwidths	2 kHz to 23.33 MHz user programmable with variable fractional output sample rate
Control & Data Interfaces	Gadget mode Ethernet via USB 2.0 USB 2.0 OTG
Control Interface	RS-232

PICO FLEXOR™ SOC MODEL

S1 DIGITAL CONFIGURATION	
SOC	Xilinx ZYNQ 7020 (85K logic cells)
Memory	Dual ARM Cortex-A9 CPU LPDDR2 512 MB CPU, 512 MB FPGA
Storage	4 GB micro-SD
S3 DIGITAL CONFIGURATION	
SOC	Xilinx ZYNQ 7045 ¹ (350K logic cells)
Memory	Dual ARM Cortex-A9 CPU LPDDR2 1GB CPU, 1GB FPGA
Storage	4 GB micro-SD

SWAP CHARACTERISTICS

PARAMETER	SPECIFICATION
Size (W x L x H)	3.0 x 5.7 x 1.3 inches - single channel 3.0 x 5.7 x 1.9 inches - dual channel
Weight	<1.5 lbs. - single channel <2.2 lbs. - dual channel
Power Consumption ² (at 10 Vdc)	/S3B25S1 9 Watts /D3B25S3 9.5 Watts

¹ Provides enhanced Gigabit Ethernet throughput.

² Based on standard FPGA load; increases with larger loads.

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INTEGRATED DEVELOPMENT ENVIRONMENT OPTION

The optional Velocity integrated development environment is an Eclipse plug-in that integrates software and FPGA application development, debugging, and deployment functionality into a single graphical environment.

- Allows portability between PicoFlexor models
- Technology and version agnostic
- Supports rebuilding OS kernels, kernel modules, and file systems for fully customizing for target applications

DEVELOPMENT AFT-END-PERIPHERAL (AEP) OPTION

This module provides high-speed backplane for application development and adds standard 1-Gig Ethernet (RJ-45) and JTAG I/O interfaces.

PICO FLEXOR™ PRODUCT LINE

NOMENCLATURE	DESCRIPTION
SI-8649A/PF/S3B25S1	Single-channel, 25 MHz BW, SOC S1
SI-8649A/PF/D3B25S1	Dual-channel, 25 MHz BW, SOC S1
SI-8649A/PF/S3B25S3	Single-channel, 25 MHz BW, SOC S3
SI-8649A/PF/D3B25S3	Dual-channel, 25 MHz BW, SOC S3
ANCILLARY ITEMS	
8649A/PF/SDK	PicoFlexor Software Developer's Kit
8649A/PF/SW/RH	PicoFlexor RedHawk Software/Firmware
8649A/PF/SW/FLEX-DDR	PicoFlexor FLEX Digital Drop Receiver with Fractional Resampler
SI-9249/FE12	Pico FE Frequency Extender to 12.4 GHz



Without the AEP module, this dual-channel PicoFlexor is ready for deployment. The AEP module is used for application development and then removed for deployment in the field.